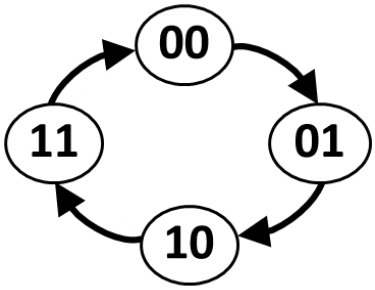
Tutorial 9 (SOLUTIONS)

NOTE THAT THERE ARE OTHER POSSIBLE SOLUTIONS TOO…

Question 1

(i) Mod-4 counter with the count sequence 0, 1, 2, 3, 0…

1) State Transition Diagram



2) Next State Table

Q_1	Q_0	Q_1^+/D_1	Q_0^+/D_0
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

$$D_0 = Q_0^+ = \overline{Q_1}\,\overline{Q_0} + Q_1\overline{Q_0} = \overline{Q_0}$$

$$D_1 = Q_1^+ = Q_1 \oplus Q_0$$

(ii) Combinational Logic

Q_1	Q_0	C_3	C_2	C_1	C_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

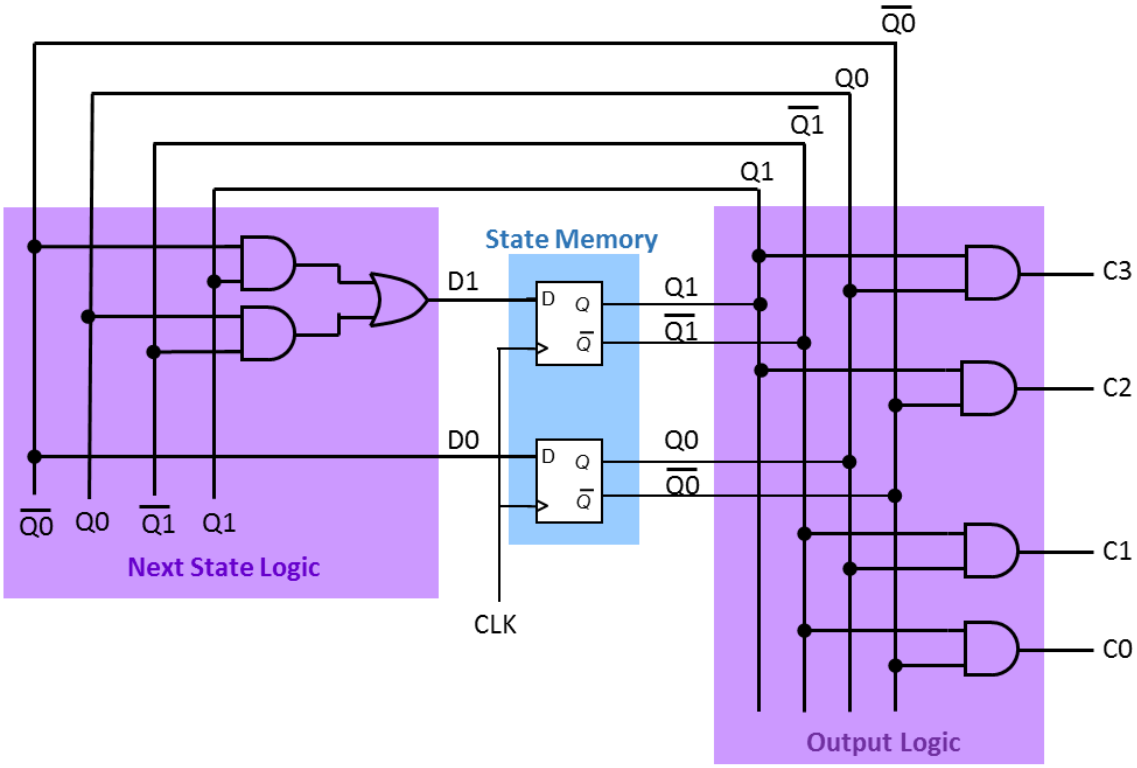
$$C_3 = Q_1Q_0$$

$$C_2 = Q_1\overline{Q_0}$$

$$C_1 = \overline{Q_1}Q_0$$

$$C_0 = \overline{Q_1}\,\overline{Q_0}$$

(iii) Circuit Realization



(iv) Comparing this implementation to T8Q2, it can be seen that while less FFs are required, more logic gates are used (complexity has increased). However, less FFs imply a smaller area or cost. Assuming the same timing characteristics for the D-FFs, the maximum operating speed of this counter would be slower due to the need to cater for additional logic gate delays from the next state logic block.

Question 2

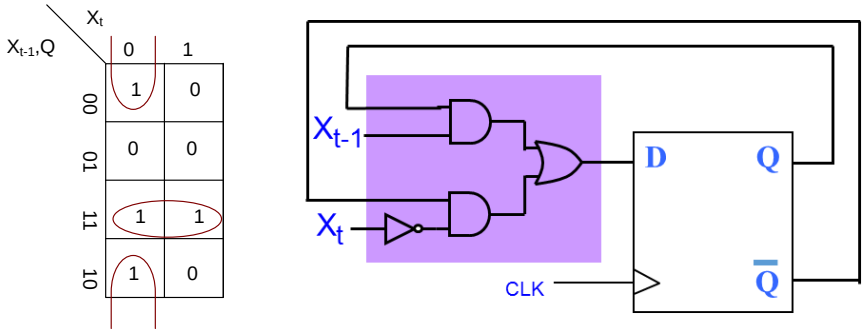
i) Design based on D-FF

The next state table (shown on the right) for X_{t-1} , X_t, Q, Q+ is derived from the problem specification.

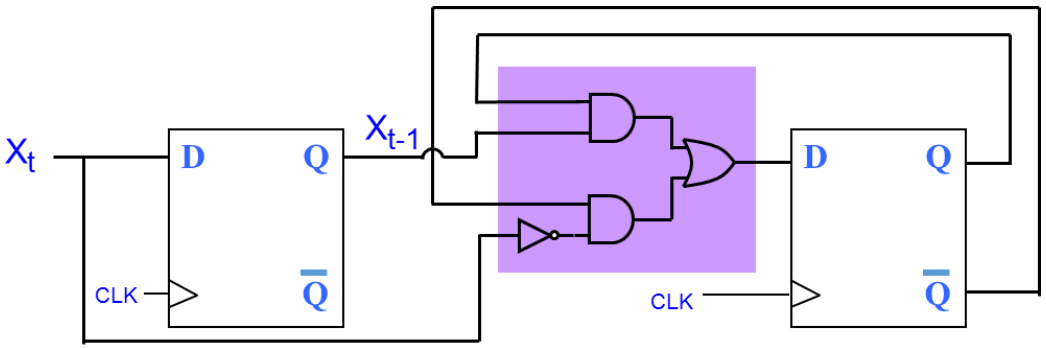
X(t)	x(t-1)	Q	Q+ / D
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Since a D-FF is being used, Q+ is also equivalent to the input of the D input of the FF. Thus, the next state table is also the truth table for the combinational circuit.

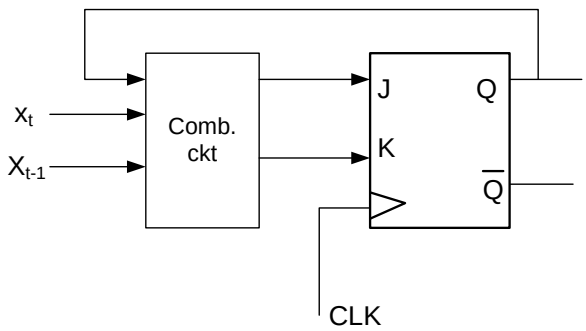
Using a D-FF, the Kmap for the combinational circuit is as below. $D = \overline{X}_t\overline{Q} + X_{t-1}Q$



Now, how to get X_{t-1} from X_t?
Simply connect X_t to the input of a D-FF, the output of the D-FF is naturally X_{t-1} .



(ii) Design based on J-K FF



Next state table :

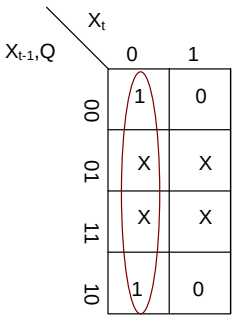
X(t)	x(t-1)	Q	Q+
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

We need to apply the excitation table of the J-K FF to obtain truth table for the combinational circuit.

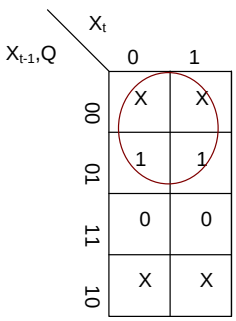
Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

The truth table for the combinational circuit is:

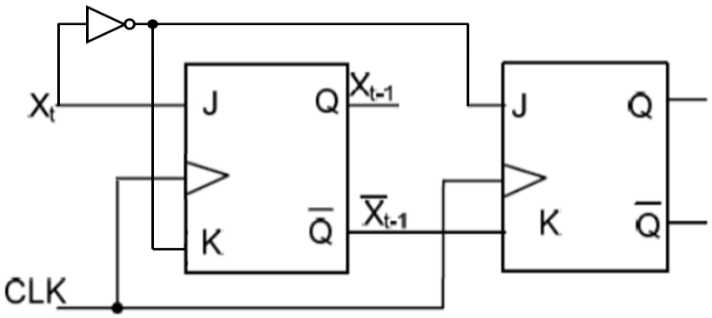
X(t)	x(t-1)	Q	Q+	J	K
0	0	0	1	1	x
0	0	1	0	x	1
0	1	0	1	1	x
0	1	1	1	x	0
1	0	0	0	0	x
1	0	1	0	x	1
1	1	0	0	0	x
1	1	1	1	x	0



$J = \overline{X}_t$



$K = \overline{X}_{t-1}$

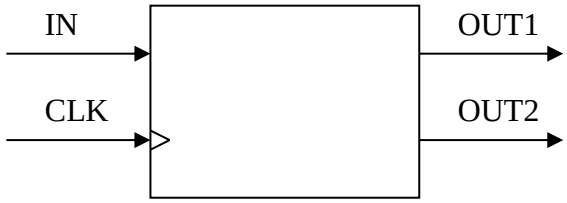


Comparison:

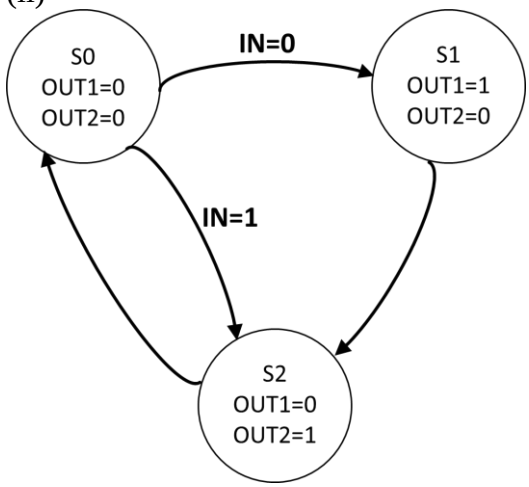
The D-FF design needs more components than J-K FF design because the D-FF is capable of only very simple behavior compared to J-K , i.e. Q+=D vs. hold, set, reset and toggle.

Question 3

(i)



(ii)



(iii)

Next State Table

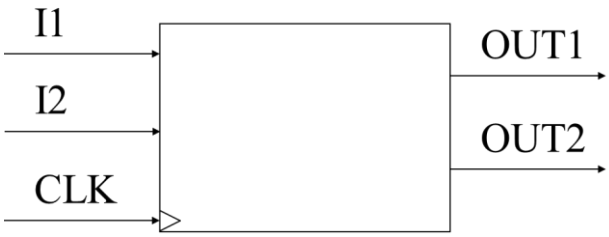
Current State	Inputs	Next State
S	**IN**	**S+**
S0	0	S1
S0	1	S2
S1	X	S2
S2	X	S0

Output Logic Table

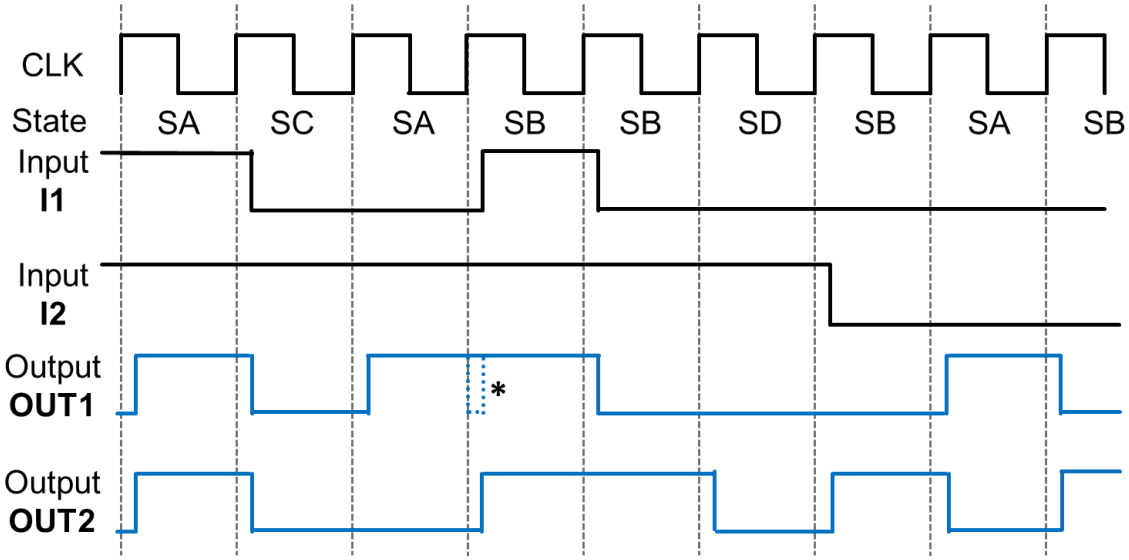
Current State	Outputs	
S	**OUT1**	**OUT2**
S0	0	0
S1	1	0
S2	0	1

Question 4

(i)



(ii) To demonstrate the effect of propagation delays, they have been included in this timing diagram. *The value of OUT1 in state SB is dependent upon the magnitude of the propagation delay vs the delay of I1 with respect to rising edge of clock. As such both solutions are accepted.



(iii)

Next State Table

Current State	Inputs		Next State
S	**I1**	**I2**	**S+**
SA	0	X	SB
SA	1	X	SC
SB	0	0	SA
SB	0	1	SD
SB	1	X	SB
SC	X	X	SA
SD	X	X	SB

Output Logic Table

Current State	Outputs	
S	**OUT1**	**OUT2**
SA	1	I1
SB	I1	1
SC	0	0
SD	0	0